REMARKS

Present Status of Application

The Office Action rejected all claims 1-20. Specifically, claim 15 was rejected under 35 U.S.C. § 101. Claims 1-20 were rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent 6,055,366 to Le et al.. In addition, claims 1 and 15 were rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent 5,050,091 to Rubin.

Applicant has amended claims 15-20 to overcome the 101 rejections. An annotated version of these claim amendments is attached hereto at Tab A. Applicant respectfully traverses the rejections under 35 U.S.C. §§ 102(e) and 102(b), and requests reconsideration and reexamination of all rejected claims 1-20.

Summary of Invention

The present invention provides a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of NFETs and PFETs and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise level values from a memory device in communication with the computer. The rules checker program

determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Rejection of claim 15 under 35 U.S.C. § 101

The Office Action rejected claim 15 under 35 U.S.C. § 101 because the claim was allegedly directed to computer code. Applicant has amended this claim to direct the claim to a computer-readable medium containing program code. Computer-readable mediums are legitimate statutory subject matter for patents. Therefore, as amended, claim 15 overcomes the rejection and the rejection should be withdrawn.

Fundamental Distinction of the Le and Rubin Patents

Applicant respectfully traverses the rejections of claim 1-20 of the present application based upon Le, for reasons that will be specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Le and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. Le, however, is wholly devoid of any teaching of ensuring the design quality of nodes for noise immunity. Indeed, the undersigned performed an electronic search of the Le patent, and the term "noise" does not appear anywhere in the text of that patent.

In contrast, Le is directed to a voltage check program that analyzes a circuit/transistor file for certain high voltage violations. In a broad sense, Le does teach the concept of a

program that checks for certain "rules" (*i.e.*, design rules) violations. However, the only rules violations that the Le patent discloses relate to high voltage violations. Indeed, Le acknowledges that it discloses only four electrical rules that are checked, stating:

> For example, various other electrical rules ***aside from the four explicitly described*** in the preferred embodiment may be checked.

(Le, col. 15, lines 62-65). However, it is well-settled law that the mere allegation that an invention is not limited to the specific embodiments disclosed therein does not expand the scope or teachings of the specification. Here, even by specific admission, Le teaches only four types of high voltage rules checks, and is absolutely devoid of any teaching of an electrical rules checking for ensuring adequate noise immunity at a gate node (or any other node for that matter). This fundamental distinction operates to prevent Le from being an anticipatory reference as to any of the claims of the present application.

Furthermore, Le specifically talks about integrating spice into an electrical rules checking program. In this regard, Le is concerned with doing checks on a circuit, whereas the present invention operates to extract parameters from a netlist. In addition, Le requires manual creation of the spice decks and checks for each individual components, whereas the present invention automatically creates these types of decks and automatic parameter extraction.

These are significant and fundamental differences between the present invention and the system and method disclosed in Le, and for at least these reasons the rejections based upon Le should be withdrawn.

With regard to the Rubin patent, that patent is even further afield of the present invention than the Le patent. In this regard, the Rubin patent discloses a design system that includes an integrated analysis and synthesis tool. However, none of the analysis tools disclosed in Rubin relate to evaluating nodes to ensure a design quality for a particular noise immunity.

This is a significant and fundamental difference between the present invention and the system and method disclosed in Rubin, and for at least this reason the rejections based upon Rubin should be withdrawn.

Le is Not Prior Art to the Present Invention

The present invention was both conceived and reduced to practice before the February 23, 1998, filing date of Le. Consequently, Le is not prior art to the present invention, and the rejection of claims 1-20 under 35 U.S.C. § 102(e) should be withdrawn on this basis alone. In this regard, a Declaration of John G. McBride (pursuant to 37 C.F.R. §1.131) is submitted herewith, which evidences (with supporting documentation) that the invention defined by the presently-pending claims was reduced to practice before February 23, 1998. On this basis alone, the rejections should be withdrawn and all claims passed to issue.

Notwithstanding, and as a separate and independent basis for the patentability of the presently-pending claims, Applicant respectfully traverses the substantive rejections of claims 1-20. The bases for this traversal are set out below.

Discussion of Specific Rejections based upon Le

Turning now to the specific rejections, the Office Action rejected claims 1-20 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 6,055,366 to Le et al. Applicant respectfully traverses this rejection for at least the reasons that follow.

First, Applicant submits that the rejections are insufficient, insofar as they do not comply with the requirements of MPEP § 707.07 *et seq.*, which requires that all rejections be stated with completeness and clarity. More specifically, MPEP § 707.07(d) requires that the grounds for rejection be "fully and clearly stated." The Office Action has failed to do this in

the present application. In this regard, in rejecting claim 1 and 20, the Office Action states only:

> As per claims 1 and 15, Le anticipated method and system apparatus for checking design rule as claimed. According to Le, the method and system for design rule checker includes a computer configured to execute a rule checker program wherein the design rule being checked for integrated circuit design having gates, gate connected in a datapath or along circuit paths including static gate characteristics, transistor parameters such as width, length, connected in device channel, etc. (see cols. 2-7).

This was the complete rejection set forth for claims 1 and 15.

First, Applicant notes that the Office Action does not even allege any teaching within Le that discloses the concept of assessing the design quality of nodes for evaluating noise immunity. However, this is a feature specifically recited in each of the independent claims. Therefore, on its face, the rejection fails to completely and sufficiently reject the claims. In addition, Applicant submits that the general reference to "cols. 2-7" is too general and vague to comply with the requirements of MPEP 707.07 *et seq.* For these reasons alone, the rejections should be withdrawn.

As a further example of the Office Action's failure to adequately reject the claims, the rejection of claim 2 merely states:

> As per claim 2, Le anticipated reading transistor design parameters for design rule check as claimed.

However, claim 2 recites:

> 2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Clearly, the rejection fails to point to the teachings within Le that allegedly disclose the claimed features of claim 2. Similar deficiencies exist in the other claim rejections as well. Therefore, these rejection should be withdrawn for these reasons. Should an ensuing Office Action be mailed, which provides more detail in this regard, such an ensuing Office Action must be made non-Final.

Claims 1-7

Independent claim 1 recites:

The Office Action rejected claims 1-7 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 6,055,366 to Le. Applicant respectfully traverses this rejection for at least the reasons that follow.

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 1 for at least the reason that Le fails to disclose or teach at least the features emphasized above.

As set forth above, Le discloses only a system that performs certain high voltage checks (see Le, col. 5, lines 54-55; col. 14, lines 34-36; and col. 15, lines 60-65). There is absolutely no teaching or disclosure within Le pertaining to the evaluation of a gate to assess whether its noise immunity is acceptable, much less to make this assessment by analyzing the widths of field effect transistors that make up the gate. These features are explicitly recited in independent claim 1. Therefore, Le cannot form a proper anticipatory reference.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 1 is misplaced and should be withdrawn. For at least these same reasons, claims 2-7, which depend from claim 1, patently define over Le as well.

Claims 8-14

The Office Action also rejected claims 8-14 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 6,055,366 to Le. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and
>
> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Le fails to disclose or teach either of the features emphasized above.

As set forth above, Le discloses only a system that performs certain high voltage checks (see Le, col. 5, lines 54-55; col. 14, lines 34-36; and col. 15, lines 60-65). There is absolutely no teaching or disclosure within Le pertaining to the evaluation of a gate to assess whether its noise immunity is acceptable, much less to make this assessment by analyzing the widths of field effect transistors that make up the gate. These features are explicitly recited in independent claim 8. Therefore, Le cannot form a proper anticipatory reference.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 8 is misplaced and should be withdrawn. For at least these same reasons, claims 9-14, which depend from claim 1, patently define over Le as well.

Claims 15-20

The Office Action also rejected claims 15-20 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 6,055,366 to Le. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 15, as amended, recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 15 for at least the reason that Le fails to disclose or teach either of the features emphasized above.

As set forth above, Le discloses only a system that performs certain high voltage checks (see Le, col. 5, lines 54-55; col. 14, lines 34-36; and col. 15, lines 60-65). There is absolutely no teaching or disclosure within Le pertaining to the evaluation of a gate to assess whether its noise immunity is acceptable, much less to make this assessment by analyzing the widths of field effect transistors that make up the gate. These features are explicitly recited in independent claim 15. Therefore, Le cannot form a proper anticipatory reference.

Accordingly, Applicant respectfully submits that the rejection of claim 15 is misplaced and should be withdrawn. Claims 16-20, which depend from claim 15 patently define over Le for at least the same reason.

Rejections based upon Rubin

The Office Action rejected only claims 1 and 15 based upon Rubin. The rejection states, in total:

> As per claims 1 and 15, Rubin anticipated method and system apparatus for checking design rule as claimed. According to Rubin, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected along circuit paths, static gate characteristics, transistor parameters such as width, length, connected channel, etc. (Abstract, "Summary of the Invention", col. 6, lines 40-48, cols. 8, 9, 12).

Applicants respectfully traverse this rejection. As noted above in connection with the rejections based upon Le, the Office Action wholly failed to even allege that Rubin discloses an evaluation of a gate for ensuring noise immunity. This is a fundamental feature of the present invention, which is specifically recited in both claims 1 and 15, and without a specific disclosure of such in Rubin, Rubin cannot properly form an anticipatory reference. Further, the undersigned notes that an electronic search was performed on the entire text of the Rubin patent and the term "noise" does not appear anywhere therein. Accordingly, the undersigned respectfully submits that Rubin cannot anticipate the present invention .

Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

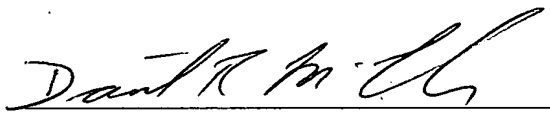
In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the

examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: 

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Annotated Version of the Claims, Highlighting Amendments Made Thereto

The following is an annotated version of the amendment made to claims 15-20, wherein underlining ("___") denotes material added to the claim and brackets ("[ ]") denotes material deleted from the claim.

15. (Once Amended) A computer-readable medium containing a rules checker computer program [embodied on a computer-readable medium], the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. (Once Amended) The computer-readable medium [program] of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

17. (Once Amended) The computer-readable medium [program] of claim 16, wherein the first code segment includes model generating code which generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the second code segment to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the third code segment determines noise levels on the first and second inputs and wherein the fourth code segment compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first model, the program determines that the gate has an acceptable immunity to noise.

18. (Once Amended) The computer-readable medium [method] of claim 17, wherein the model generating code generates a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the second code segment to access a third and fourth threshold values stored in the memory device, wherein the third code segment determines noise levels on the first and second inputs when the first and second inputs are low and wherein the fourth code segment compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the program determines that the gate has an acceptable noise immunity.

19. (Once Amended) The computer-readable medium [program] of claim 18, wherein the model generating code generates a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the second code segment to access fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the fifth threshold value, and wherein when the first input is low, the third code segment determines

the noise level on the first input and wherein the fourth code segment compares the determined noise level to the sixth threshold value, the fourth code segment using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the program determines that the gate has an acceptable noise immunity.

20. (Once Amended) The computer-readable medium [program] of claim 19, wherein the model generating code generates a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the second code segment to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the seventh threshold value, and wherein when the second input is high, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the eighth threshold value, the fourth code segment using the results of the comparison to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the program determines that the gate has an acceptable noise immunity.